

## 74F794 8-Bit Register with Readback

### General Description

The 74F794 is an 8-bit register with readback capability designed to store data as well as read the register information back onto the data bus. The I/O bus (D bus) has 3-STATE outputs. Current sinking capability is 64 mA on both the D and Q busses.

Data is loaded into the registers on the LOW-to-HIGH transition of the clock (CP). The output enable ( $\overline{OE}$ ) is used to enable data on  $D_0$ - $D_7$ . When  $\overline{OE}$  is LOW, the output of the registers is enabled on  $D_0$ - $D_7$ , enabling D as an output bus. When OE is HIGH,  $D_0$ - $D_7$  are inputs to the registers configuring D as an input bus.

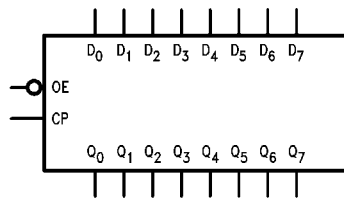
### Features

- 3-STATE outputs on the I/O port
- D and Q output sink capability of 64 mA
- Functionally and pin equivalent to the 74LS794

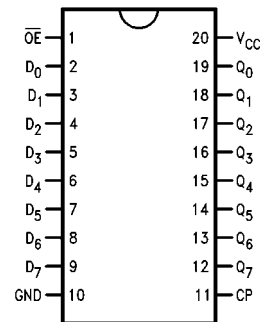
### Ordering Code:

Order Number	Package Number	Package Description
74F794PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

### Logic Symbol



### Connection Diagram



### Input Loading/Fan-Out

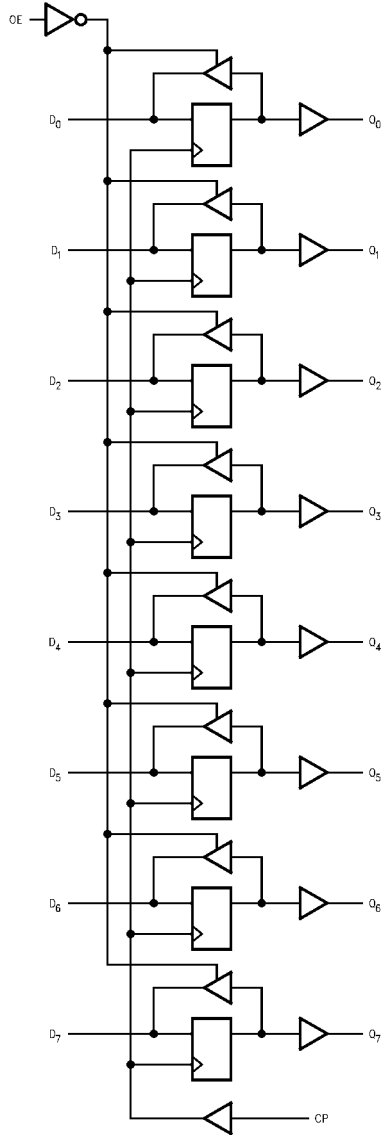
Pin Names	Description	HIGH/LOW	
		(U.L.)	Current
$\overline{OE}$	Output Enable Input	1.0/1.0	20 $\mu$ A/-0.6 mA
CP	Clock Pulse Inputs	1.0/1.0	20 $\mu$ A/-0.6 mA
$D_0$ - $D_7$	D Bus Inputs/ 3-STATE Outputs	3.5/1.083	70 $\mu$ A/-650 $\mu$ A
$Q_0$ - $Q_7$	Q Bus Outputs	750/106.6	-15 mA/64 mA

### Truth Table

Inputs		Outputs	
CP	$\overline{OE}$	Q	D
L or H or $\downarrow$	L	$Q_n$	Output, Q
L or H or $\downarrow$	H	$Q_n$	Input
$\uparrow$	L	$Q_n$	Output, Q (Note 1)
$\uparrow$	H	D	Input

**Note 1:** In this case the output of the register is clocked to the inputs and the overall Q output is unchanged at  $Q_n$ .

### Logic Diagram



**Absolute Maximum Ratings** (Note 2)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55° to +125°C
Junction Temperature under Bias	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 3)	-0.5V to +7.0V
Input Current (Note 3)	-30 mA to +5.0 mA
ESD Last Passing Voltage (Min)	4000V
Voltage Applied to Output	
In HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
3-STATE Output	-0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	Twice the Rated I <sub>OL</sub> (mA)

**Recommended Operating Conditions**

Free Air Ambient Temperature	0°C to 70°C
Supply Voltage	+4.5V to +5.5V

**Note 2:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

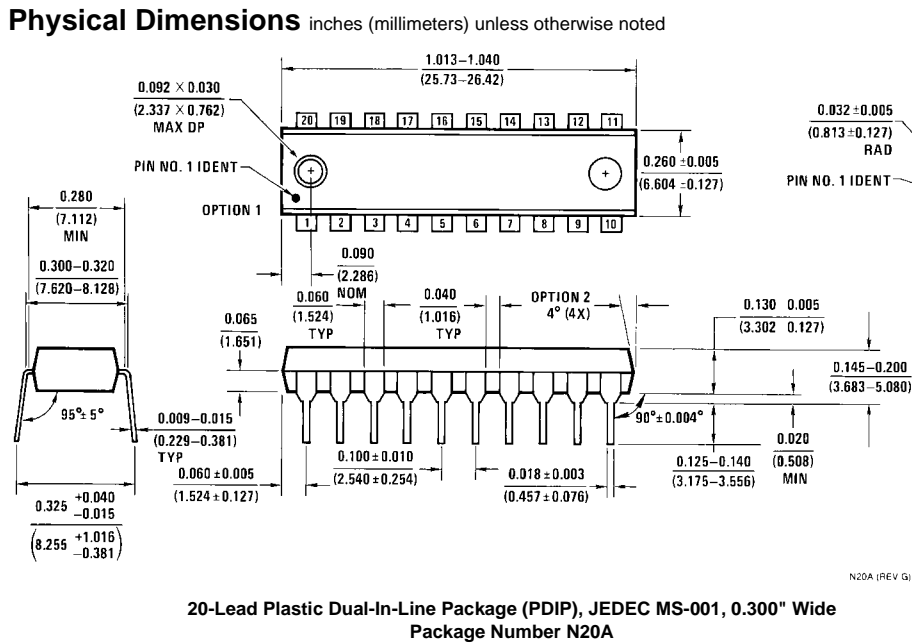
**Note 3:** In this case the output of the register is clocked to the inputs and the overall Q output is unchanged at Q<sub>n</sub>.

**Note 4:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics** over Operating Temperature Range unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.4	2.8		V	Min	I <sub>OH</sub> = -3 mA I <sub>OH</sub> = -15 mA
V <sub>OL</sub>	Output LOW Voltage		0.45	0.55	V	Min	I <sub>OL</sub> = 64 mA
I <sub>IH</sub>	Input HIGH Current			5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7.0	μA	Max	V <sub>IN</sub> = 7.0V ( $\overline{OE}$ , CP)
I <sub>BVIT</sub>	Input HIGH Current Breakdown (I/O)			0.5	mA	Max	V <sub>IN</sub> = 5.5V (D <sub>n</sub> )
I <sub>CEX</sub>	Output HIGH Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V ( $\overline{OE}$ , CP)
I <sub>OS</sub>	Output Short-Circuit Current	-100		-225	mA	Max	V <sub>OUT</sub> = 0V
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current			70	μA	Max	V <sub>OUT</sub> = 2.7V (D <sub>n</sub> )
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current			-650	μA	Max	V <sub>OUT</sub> = 0.5V (D <sub>n</sub> )
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Circuit Leakage Current			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>ZZ</sub>	Bus Drainage Test			100	μA	0.0	V <sub>OUT</sub> = 5.25V
I <sub>CCH</sub>	Power Supply Current			65	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current			80	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current			80	mA	Max	V <sub>O</sub> = HIGH Z

AC Electrical Characteristics							
Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF		Units
		Min	Typ	Max	Min	Max	
f <sub>MAX</sub>	Maximum Clock Frequency	90			90		MHz
t <sub>PLH</sub>	Propagation Delay	2.5		7.0	2.5	8.0	ns
t <sub>PHL</sub>	CP to Q <sub>n</sub>	2.5		8.0	2.5	9.0	
t <sub>PZH</sub>	Output Enable Time	2.3		8.5	2.0	9.0	ns
t <sub>PZL</sub>		2.0		10.0	2.0	10.5	
t <sub>PHZ</sub>	Output Disable Time	1.0		7.0	1.0	8.0	ns
t <sub>PLZ</sub>		1.0		7.0	1.0	8.0	
t <sub>S</sub> (H)	Setup Time, HIGH or LOW	4.0			4.0		ns
t <sub>S</sub> (L)	Bus to Clock	4.0			4.0		
t <sub>H</sub> (H)	Hold Time, HIGH or LOW	1.5			1.5		ns
t <sub>H</sub> (L)	Bus to Clock	1.5			1.5		
t <sub>W</sub> (H)	Clock Pulse Width	5.8			5.8		ns
	HIGH or LOW	5.8			5.8		



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